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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08 December 2009</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1,4-9,11,12,14,16-19,31,34-39,41,42,44,46-49 and 64-66</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1, 4-9, 11-12, 14, 16-19, 31, 34-39, 41-42, 44, 46-49, 64-66</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

This Action is in response to communications filed 12/08/2009.

Claims 1, 4-9, 11-12, 14, 16-19, 31, 34-39, 41-42, 44, 46-49, 64-66 are pending.

Claims 2-3, 10, 13, 15, 32-33, 40, 43, 45 and 60-63 were cancelled previously.

Claims 20-30 and 50-59 were withdrawn previously.

Re-opening Prosecution After Appeal Brief

In view of the appeal brief filed on 12/08/2009, PROSECUTION IS HEREBY
REOPENED. A new grounds of rejections is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following
two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37
CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an
appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee
can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have
been increased since they were previously paid, then appellant must pay the difference between
the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing
below:

Response to Arguments

Applicant's arguments with respect to claims above have been considered but are moot in view of the new ground(s) of rejection.

In the appeal Brief, applicant admitted that Pettey does teach, in column 14, the use of a response descriptor (the SGL) for responding to an incoming read request packet, e.g. brief, pg. 16: 1st paragraph.

Initially, appellant specification, e.g. pg. 3: 3rd paragraph to pg. 4 3rd paragraphs, discloses that:

> "To handle the dual role of requester and responder, IB HCAs known in the art typically have separate, independent transmit and receive hardware structures. An example…This device features a dual pipeline…
> It is an object of the present invention to provide improved devices and methods for interfacing a host processor to a network…it is a further object of some aspects of the present invention to provide a HCA that performs RDMA read and write operations efficiently, with reduced hardware requirements relative to devices known in the art…"

Stated another way, the present invention and independent claim 1 are mere improvements of known prior art. The improvement includes **reducing** hardware structures by introducing a common/single/shared module or engine such as gather engine.

In response, first, it should be noted that it is well known in the art that when all of the essential elements of the claim(s) except integration of parts are found in the reference(s), the mere unity of parts is not considered to be an inventive concept. In re Lockhart, 90 USPQ 214 (CCPA 1951), In re Murray, 19 C.C.P.A. 739, 53 F.2d 541, 11 USPQ 155; In re Zabel et al., 38 C.C.P.A. 832, 186 F.2d 735, 88 USPQ 367.

Accordingly, at the time of the invention, it would have been obvious to one of ordinary skill in the arts to integrate the plurality of functions, engines and/or modules to a single engine,

since it is well known in the art that when all of the essential elements of the claim(s) except

integration of parts are found in the reference(s), the mere unity of parts is not considered to be

an inventive concept, as evidenced by the prima facie case of obviousness, set forth herein.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1.   Claims 1, 4-9, 11-12, 14, 16, 17-19, 31, 34-39, 41-42, 44, 46-49, 64-66 (different from

the original claims) are provisionally rejected on the ground of nonstatutory obviousness-type

double patenting as being unpatentable over claims 1-10, 12-17, 19-23 (different from the

original claims) of copending Application No. 11/348,259 in view of Pettey et al. (hereinafter

Pettey et al., U. S. Patent No. 6,594,712 B1).

As per claim 1, claim 1 of Co-pending '259 discloses each and every limitation of claim 1 of present application.

However, co-pending claim 1 does not disclose outgoing packet generator comprising a gather engine which is coupled to gather both the write data and the read data from the system memory, and wherein to submit a request, the host processor writes a request descriptor indicative of the write data to a second memory location.

Pettey discloses a gather engine which is coupled to gather write data from the system memory and wherein to submit a request, the host processor writes a request descriptor indicative of the write data to a second memory location (col. 14 L10-67, fig. 2 item #218, fig. 7B: the WQE are stored in local memory, separate from the TCA, and col. 25 L10-26).

Therefore, it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Co-pending '259 in view of Pettey in order to include a gather engine that gathers both the write data and read data in response to write requests and incoming read requests by reading the WQEs corresponding to the write data and read data. See In re Lockhart, 90 USPQ 214 (CCPA 1951), In re Murray, 19 C.C.P.A. 739, 53 F.2d 541, 11 USPQ 155; In re Zabel et al., 38 C.C.P.A. 832, 186 F.2d 735, 88 USPQ 367 (The mere unity of parts is not considered to be an inventive concept).

Claim 8 of present application is similar to claim 2 of co-pending application.

Independent claim 31 is rejected for the same reasons as set forth above.

This is a provisional obviousness-type double patenting rejection.

Please note that the listing above is not intended to be exhaustive and is provided an exemplary.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c)

and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2.   Claims 1, 4-5, 7, 9, 12, 14, 16-19, 31, 34-38, 42, 44, 46-49 and 64-66 are rejected under

35 U.S.C. 103(a) as being obvious over Pettey et al. (hereinafter Pettey et al., U. S. Patent No.

6,594,712 B1) in view of Pettey (US 2003/0014544 A1).

As per claim 1, Pettey et al. discloses a network interface adapter (fig. 3 item #202:

Channel adapter), comprising:

a host interface for coupling to a host processor (fig. 3 item #214: interfaces for

coupling);

an outgoing packet generator, adapted to generate an outgoing request packet for delivery

to a remote responder responsive to a request submitted by the host processor via the host

interface (col. 7 L65 to col. 8 L7, col. 14 L20-39, fig. 3 item #306: Bus router generates the packets);

a network output port, coupled to receive the request packet from the output packet generator, so as to transmit the outgoing request packet over a network to the remote responder (col. 9 L1-5, fig. 3 item #308: network interfaces);

a network input port, for coupling to the network so as to receive an incoming response packet from the remote responder, in response to the outgoing request packet sent thereto, and further to receive an incoming request packet sent by a remote requester (fig. 3 item #308: network interfaces and fig. 2 item #204);

an incoming packet processor, coupled to the network input port so as to receive and process both the incoming response packet and the incoming request packet, and further coupled to cause the outgoing packet generator, responsive to the incoming request packet, to generate in addition to the outgoing request packet, an outgoing response packet for transmission via the network output port to the remote requester (col. 10 L4-9, col. 14 L40-54 and fig. 3 item #306: Bus router processes packets as well),

wherein the outgoing request packet comprises an outgoing write request packet containing write data taken from a system memory accessible via the host interface (fig. 18a: describes the process of RDMA WRITE operation; fig. 16: shows the I/O WRITE operation, col. 11 L18-27, col. 13 L18-57),

wherein the outgoing response packet comprises an outgoing read response packet containing read data taken from the system memory in response to the incoming request packet (fig. 18a, fig. 16, col. 13 L58 to col. 14 L9), and

wherein the incoming request packet comprises an incoming read request packet specifying data to be read from a system memory accessible via the host interface (fig. 15: describes an incoming read request packet, col. 11 L17-67, col. 13 L58 to col. 14 L9, L40-65 and col. 15 L65 to col. 16 L6);

wherein the incoming packet processor is adapted to write a response descriptor to a first memory location, in a memory separate from the network interface adapter, indicating the data to be read from the system memory responsive to the incoming read request packet (col. 14 L10-67, fig. 2 item #218, fig. 7B: the WQE are stored in local memory, separate from the TCA, and col. 25 L10-26);

wherein the outgoing packet processor is adapted to read the response descriptor from the first memory location and, responsive thereto, to read the indicated data and to generate outgoing response packet containing the indicated data (col. 9 L1-5, col. 11 L54 to col. 12 L67, col. 22 L39-67).

wherein to submit the request, the host processor writes a request descriptor indicative of the write data to a second memory location (col. 11 L18 to col. 12 L45 and fig. 7b).

However, Pettey et al. does not explicitly disclose the GATHER engine which is coupled to gather both the write data and the read data from the system memory for inclusion in the respective outgoing packets and a process adapted to read information from the descriptors and to gather the read data and the write data responsive thereto (i.e. Pettey does not explicitly disclose using a shared/single module or engine to gather both the write data and read data).

Pettey discloses the GATHER engine which is coupled to gather both the write data and the read data from the system memory for inclusion in the respective outgoing packets and a

process adapted to read information from the descriptors and to gather the read data and the write data responsive thereto (fig. 8: HCA, pg. 12 [105-107] to pg. 13 [108]: receiving RDMA read command from target adapter and responding, by the single/shared/common transport engine based on the response WQE 858 in the accelerated send queue, pg. 12 [102]: transport engine processing the WQEs).

Therefore, it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey et al in view of Pettey (hereinafter Pettey-Pettey) in order to gather both the write data and the read data from the system memory for inclusion in the respective outgoing packets.

One of ordinary skilled in the art would have been motivated because it would have enabled transmitting the message data to the target adapter (Pettey: pg. 13 [0108]) (In re Lockhart, 90 USPQ 214 (CCPA 1951), In re Murray, 19 C.C.P.A. 739, 53 F.2d 541, 11 USPQ 155; In re Zabel et al., 38 C.C.P.A. 832, 186 F.2d 735, 88 USPQ 367: mere unity of parts, i.e. integrating into a single module).

As per claim 4, Pettey-Pettey discloses the interface adapter wherein the outgoing packet generator comprises a plurality of schedule queues (Pettey et al.: fig. 7a block #108: Queue Pairs), and is adapted to generate the outgoing request packet (Pettey: fig. 16) and the outgoing response packet responsive to respective entries placed in the schedule queues of the plurality of schedule queues (Pettey et al.: col. 11 L18-53: WQEs are placed in the respective queue pairs, col. 14 L10-54, fig. 18a item #1808, 1822, fig. 22a item #2224, 2226 and fig. 15).

As per claim 5, Pettey-Pettey discloses the interface adapter wherein the network input and output ports are adapted to receive and send the incoming and outgoing packets,

respectively, over a plurality of transport service instances (i.e. over queue pairs), and wherein the outgoing request packet and the outgoing response packet are associated with respective instances among the plurality of transport service instances (Pettey et al.: fig. 7a item #108: send/receive queues), and wherein the outgoing packet generator is adapted to assign the transport service instances of the plurality of transport service instances to the schedule queues of the plurality of schedule queues based on service parameters of the instances (Pettey: col. 11 L1-21: plurality of QPs exist and/or are configured/assigned based on send/receive functions), and to place the entries in the schedule queues corresponding to the transport service instances with which the incoming and outgoing packets are associated (Pettey et al.: col. 8 L2-26, col. 11 L1-36: placing WQEs and col. 14 L10-54).

As per claim 7, Pettey-Pettey discloses an adapter wherein the transport service instances comprise queue pairs (Pettey et al: col. 11 L1-50).

As per claim 9, Pettey-Pettey discloses an adapter wherein the incoming request packet comprises a write request packet carried over the network on a reliable transport service, and wherein responsive to the incoming write request packet, the incoming packet processor is adapted to add an entry to the entries placed in the queues, such that responsive to the entry, the outgoing packet generator generates an acknowledgement packet (Pettey et al.: col. 11 L1-58).

As per claim 12, Pettey-Pettey discloses an adapter wherein the incoming packet processor is configured so that when it receives an incoming write request packet containing write data to be written to a system memory accessible via the host interface before receiving the incoming read request packet, it prevents execution of the read response work item or response

descriptor until the write data have been written to the system memory (Pettey: col. 21 L12 to col. 22 L6).

As per claim 14, Pettey-Pettey discloses an adapter wherein the outgoing packet generator is adapted, upon generating the outgoing request packet, to notify the incoming packet processor to await the incoming response packet so as to write a completion message to the host interface when the awaited packet is received (Pettey et al.: col. 20 L17-32).

As per claim 16, Pettey-Pettey discloses an adapter wherein the incoming read request packet is **one of a** plurality of incoming read request packets, and wherein the incoming packet processor is adapted to write a list of corresponding response descriptor to the first memory location each said response descriptor indicating the data to be read from the system memory responsive to the corresponding incoming read request packet, responsive to which the outgoing packet processor is adapted to generate the outgoing response packet as part of a sequence of such packets (Pettey et al.: fig. 19a, fig. 20 and fig. 9; col. 23 L20 to col. 24 L27; col. 11 L18-37, fig. 7b, fig. 2 and col. 14 L10-20).

As per claim 17, Pettey-Pettey discloses an adapter wherein the network input and output ports are adapted to receive and send the incoming and outgoing packets, respectively, over a plurality of transport service instances, and wherein the incoming packet processor is adapted to prepare the list of the response descriptors for each of the instances as a part of a response database held for the plurality of the instances in common (Pettey: fig. 8: HCA, pg. 12 [105-107] to pg. 13 [108]: receiving RDMA read command from target adapter and responding, by the single/shared/common transport engine based on the response WQE 858 in the accelerated send queue, pg. 12 [102]: transport engine processing the WQEs).

As per claim 18, Pettey-Pettey discloses an adapter wherein the transport service instances comprise queue pairs (Pettey et al.: col. 11 L1-17).

As per claim 19, Pettey-Pettey discloses the adapter wherein the request comprises a write request, which is submitted by the host processor by generating a request descriptor indicating further data to be read from the system memory for inclusion in the outgoing packet (fig. 10), and wherein the output packet generator is adapted to read the request descriptor and, responsive thereto, to generate the outgoing request packet as a write request packet containing the indicated further data (Pettey et al.: fig. 18a item #1832; col. 12 L58 to col. 13 L18, col. 15 L17-31 and fig. 16).

As per claim 64, Pettey-Pettey discloses an adapter wherein the memory separate from the network interface is the system memory (Pettey et al.: fig. 2 item #218).

As per claim 65, Pettey-Pettey discloses the adapter wherein the incoming read request packet is a RDMA read request packet and wherein the response descriptor is a quasi-WQE (i.e. work item; Pettey et al.: fig. 7b, col. 11 L1-53; Pettey: fig. 8: HCA, pg. 12 [105-107] to pg. 13 [108]: receiving RDMA read command from target adapter and responding, by the single/shared/common transport engine based on the response WQE 858 in the accelerated send queue, pg. 12 [102]: transport engine processing the WQEs).

As per claims 31, 34-38, 42, 44, 46-49 and 66, they do not teach or further define over the limitations in claims 1, 4-7, 9, 12, 14, 16-19 and 64-65. Therefore claims 31, 34-38, 42, 44, 46-49 and 66 are rejected for the same reasons as set forth in claims 1, 4-7, 9, 12, 14, 16-19 and 64-65.

3.   Claims 6, 8, 11, 39 and 41 are rejected under **35 U.S.C. 103(a)** as being obvious over

Pettey et al. (hereinafter Pettey, U. S. Patent No. 6,594,712 B1) in view of Gasbarro et al.

(hereinafter Gasbarro, U. S. Patent No. 6,948,004 B2).

As per claim 6, Pettey-Pettey discloses the adapter of claim 5 as set forth above, wherein

the outgoing packet generator comprises one or more execution engines, which are adapted to

generate the outgoing request packet and the outgoing response packet responsive to a list of

work items respectively associated with each of the transport service instances (Pettey et al: col.

11 L18-53, col. 14 L10-54) and assigning the transport service instances of the plurality of

transport service instances to the one or more execution engines for execution of the work items

(Pettey et al: col. 11 L1-21: plurality of QPs exist and/or are configured/assigned based on

send/receive functions).

However, Pettey-Pettey does not disclose a scheduler, which is coupled to select the

entries from the plurality of schedule queues.

Gasbarro discloses an adapter comprising a scheduler for scheduling the next virtual

interface to the context manager and supporting priority of traffic for data packets associated

with send queue and receive queue of the work queue pair, i.e. selecting the work items based on

priority (col. 15 L50-58).

Therefore, it would have been obvious to a person of ordinary skilled in the art at the time

the invention was made to modify Pettey-Pettey in view Gasbarro, in order to include a scheduler

for selecting the entries from the queues and to assign the instances to the execution engines for

execution of the work items responsive to the service parameters.

One of ordinary skilled in the art would have been motivated because a scheduler would have supported the priority of traffic for data packets associated with send queue and receive queue of the work queue pair (Gasbarro, col. 15 L50-55).

As per claim 8, Pettey-Pettey discloses the adapter of claim 4, wherein the outgoing packet generator comprises one or more control registers to which the host processor and incoming packet processor write in order to place the entries in the queues (Pettey et al.: col. 17 L20-56).

However, Pettey-Pettey does not explicitly disclose the one or more register to be a doorbell registers.

Gasbarro explicitly discloses a channel adapter comprising one or more doorbell registers (col. 15 L20-50).

Therefore, it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey-Pettey in view of Gasbarro, in order to replace the one or more control registers with the doorbell registers, since Gasbarro teaches and discloses the usage of doorbell registers.

One of ordinary skilled in the art would have been motivated because doorbell registers allows software the capability to enable automatic event generation, and making doorbell registers memory mapped allows applications the ability to write those registers thereby controlling event generation (Gasbarro: col. 15 L20-32).

As per claim 11, Pettey-Pettey discloses the adaptor of claim 1, including the process of receiving a read request (Pettey et al.: fig. 15 item #1000); the process of receiving a write

request (fig. 16 item #1000); and the process of conveying or sending the write data to the host interface (fig. 15 item #1100).

However, Pettey-Pettey does not disclose the process of receiving an incoming write request packet containing write data to be written to a system memory accessible via the host interface after receiving the incoming read request packet, and the process of conveying the write data to the host interface without waiting for execution of the response descriptor.

Gasbarro discloses the adaptor which supports the priority of traffic for data packets associated with send Queue and Receive Queue of the work queue pair, i.e. selecting the work items for processing based on priority (col. 15 L50-58; See also applicant specification, pg. 26: inherent IB convention).

Therefore, it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey-Pettey (i.e. modify Pettey's figure 15 and 16 so that the incoming packet processor of the adapter (see the rejected claim 1) is configured so that the write request work queue entry is executed first based on priority with respect to read response work queue entry or response descriptor) in order to convey the write data to the host interface without waiting for execution of the read response work item.

One of ordinary skilled in the art would have been motivated because it would enable processing the prioritized packets (Gasbarro: col. 15 L50-58).

4.   Claims 1 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Applicant Admitted Prior art (AAPA).

As per claim 1, AAPA discloses a network interface adapter (specification, pg. 1-4:

Background of Invention), comprising:

a host interface for coupling to a host processor (pg. 1-4: Background of Invention);

an outgoing packet generator, adapted to generate an outgoing request packet for delivery

to a remote responder responsive to a request submitted by the host processor via the host

interface (pg. 1-4: Background of Invention);

a network output port, coupled to receive the request packet from the output packet

generator, so as to transmit the outgoing request packet over a network to the remote responder

(pg. 1-4: Background of Invention);

a network input port, for coupling to the network so as to receive an incoming response

packet from the remote responder, in response to the outgoing request packet sent thereto, and

further to receive an incoming request packet sent by a remote requester (pg. 1-4: Background of

Invention);

an incoming packet processor, coupled to the network input port so as to receive and

process both the incoming response packet and the incoming request packet, and further coupled

to cause the outgoing packet generator, responsive to the incoming request packet, to generate in

addition to the outgoing request packet, an outgoing response packet for transmission via the

network output port to the remote requester (pg. 1-4: Background of Invention);

wherein the outgoing request packet comprises an outgoing write request packet containing write data taken from a system memory accessible via the host interface (pg. 1-4: Background of Invention);

wherein the outgoing response packet comprises an outgoing read response packet containing read data taken from the system memory in response to the incoming request packet (pg. 1-4: Background of Invention); and

wherein the incoming request packet comprises an incoming read request packet specifying data to be read from a system memory accessible via the host interface (pg. 1-4: Background of Invention);

wherein the incoming packet processor is adapted to write a response descriptor to a first memory location, in a memory separate from the network interface adapter, indicating the data to be read from the system memory responsive to the incoming read request packet (pg. 1-4: Background of Invention);

wherein the outgoing packet generator is adapted to read the response descriptor from the first memory location and, responsive thereto, to read the indicated data and to generate outgoing response packet containing the indicated data (pg. 1-4: Background of Invention);

wherein the outgoing packet generator comprises gather engine which is coupled to gather write data from the system memory for inclusion in the respective outgoing packets (pg. 1-4: Background of Invention) and a separate gather engine which is coupled to gather the read data from the system memory for inclusion on the respective outgoing packets (pg. 1-4: Background of Invention: The HCA serves both as a requestor and responder using separate hardware);

wherein to submit the request, the host processor writes a request descriptor indicative of the write data to a second memory location (pg. 1-4: Background of Invention: Generally HCA uses WQEs to post work requests) and wherein the gather engine is adapted to read information from the response descriptor and a separate gather engine adapted to read information from the request descriptor and to gather the read data and write data (pg. 1-4: Background of Invention: The HCA serves as both the requestor and responder);

However, AAPA does not disclose the GATHER engine which is coupled to gather both the write data and the read data from the system memory for inclusion in the respective outgoing packets and a process adapted to read information from the descriptors and to gather the read data and the write data responsive thereto (i.e. AAPA does not explicitly disclose using a shared/single module or engine to gather both the write data and read data).

But, at the time of the invention, it would have been obvious to one of ordinary skill in the arts to integrate the plurality of functions, engines and/or modules to a single engine, since it is well known in the art that when all of the essential elements of the claim(s) except integration of parts are found in the reference(s), the mere unity of parts is not considered to be an inventive concept. See In re Lockhart, 90 USPQ 214 (CCPA 1951), In re Murray, 19 C.C.P.A. 739, 53 F.2d 541, 11 USPQ 155; In re Zabel et al., 38 C.C.P.A. 832, 186 F.2d 735, 88 USPQ 367 (The mere unity of parts is not considered to be an inventive concept.

As per claim 31, it does not teach or further define over the limitations in claim 1. Therefore, claim 31 is rejected for the same reasons as set forth in claim 1.

Additional References

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.   Beukema et al., U. S. Patent No. 6,578,122 B2: Using an Access Key to protect and point to regions in windows for infiniband.

b.   Avery, U. S. Patent No. 6,611,883 B1: Method and Apparatus for Implementing PCI DMA speculative prefetching in a message passing queue oriented bus system.

c.   Thomas et al., U. S. Patent No. 5,922,046: Method and Apparatus for avoiding control reads in a network node.

d.   Coffman et al., U. S. Patent No. 6,718,370 B1: Completion Queue management mechanism.

e.   Pettey, US 7,149,817: Infiniband TM Work Queue to TCP/IP translation.

Conclusion

The teachings of the prior art should not be restricted and/or limited to the citations by columns and line numbers, as specified in the rejection. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in its entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

In the case of amendments, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and support, for ascertaining the metes and bounds of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAMAL B. DIVECHA whose telephone number is (571)272-5863. The examiner can normally be reached on Increased Flex Work Schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on 571-272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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